# BP9960

**N-CHANNEL ENHANCEMENT MODE POWER MOSFET**

| | |
|---|---|
| $BV_{DSS}$ | 40V |
| $R_{DS(ON)}$ | 20mΩ |
| $I_D$ | 7.8A |

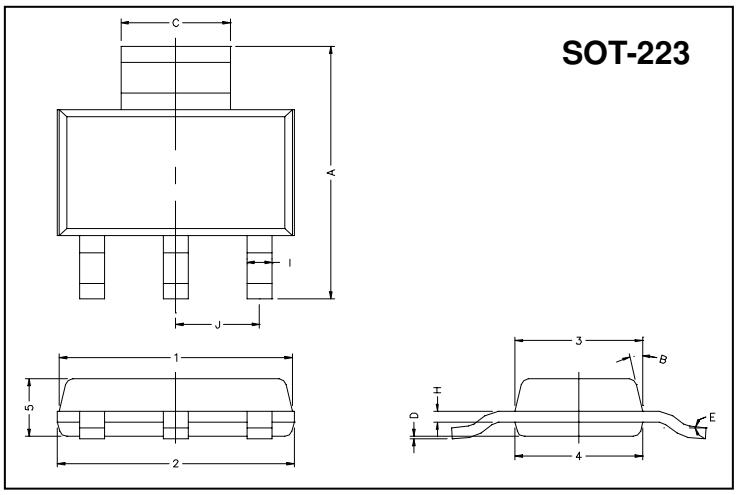
## Description

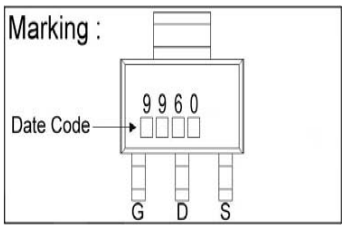
The BP9960 provide the designer with the best combination of fast switching, ruggedized device design, ultra low on-resistance and cost-effectiveness.

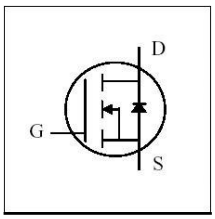
## Features

*Low On-Resistance
*Fast Switching Speed

## Package Dimensions




| REF. | Millimeter | | REF. | Millimeter | |
|---|---|---|---|---|---|
| | Min. | Max. | | Min. | Max. |
| A | 6.70 | 7.30 | B | 13°TYP. | |
| C | 2.90 | 3.10 | J | 2.30 REF. | |
| D | 0.02 | 0.10 | 1 | 6.30 | 6.70 |
| E | 0° | 10° | 2 | 6.30 | 6.70 |
| I | 0.60 | 0.80 | 3 | 3.30 | 3.70 |
| H | 0.25 | 0.35 | 4 | 3.30 | 3.70 |
| | | | 5 | 1.40 | 1.80 |

## Absolute Maximum Ratings

| Parameter | Symbol | Ratings | Unit |
|---|---|---|---|
| Drain-Source Voltage | $V_{DS}$ | 40 | V |
| Gate-Source Voltage | $V_{GS}$ | ±20 | V |
| Continuous Drain Current[3] | $I_D$ @$T_A$=25℃ | 7.8 | A |
| Continuous Drain Current[3] | $I_D$ @$T_A$=70℃ | 6.2 | A |
| Pulsed Drain Current[1] | $I_{DM}$ | 20 | A |
| Total Power Dissipation | $P_D$ @$T_A$=25℃ | 2.7 | W |
| Linear Derating Factor | | 0.02 | W/℃ |
| Operating Junction and Storage Temperature Range | Tj, Tstg | -55 ~ +150 | ℃ |

## Thermal Data

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Thermal Resistance Junction-ambient[3] Max. | Rthj-amb | 45 | ℃/W |

## Electrical Characteristics (Tj = 25℃ unless otherwise specified)

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Drain-Source Breakdown Voltage | $BV_{DSS}$ | 40 | - | - | V | $V_{GS}$=0, $I_D$=250uA |
| Breakdown Voltage Temperature Coefficient | $\triangle BV_{DSS}/\triangle Tj$ | - | 0.032 | - | V/℃ | Reference to 25℃, $I_D$=1mA |
| Gate Threshold Voltage | $V_{GS(th)}$ | 1.0 | - | 3.0 | V | $V_{DS}$=$V_{GS}$, $I_D$=250uA |
| Forward Transconductance | $g_{fs}$ | - | 25 | - | S | $V_{DS}$=10V, $I_D$=7A |
| Gate-Source Leakage Current | $I_{GSS}$ | - | - | ±100 | nA | $V_{GS}$= ±20V |
| Drain-Source Leakage Current(Tj=25℃) | $I_{DSS}$ | - | - | 1 | uA | $V_{DS}$=40V, $V_{GS}$=0 |
| Drain-Source Leakage Current(Tj=70℃) | | - | - | 25 | uA | $V_{DS}$=32V, $V_{GS}$=0 |
| Static Drain-Source On-Resistance | $R_{DS(ON)}$ | - | - | 20 | m | $V_{GS}$=10V, $I_D$=7A |
| | | - | - | 32 | | $V_{GS}$=4.5V, $I_D$=5A |
| Total Gate Charge[2] | $Q_g$ | - | 14.7 | - | nC | $I_D$=7A<br>$V_{DS}$=20V<br>$V_{GS}$=4.5V |
| Gate-Source Charge | $Q_{gs}$ | - | 7.1 | - | | |
| Gate-Drain (“Miller”) Change | $Q_{gd}$ | - | 6.8 | - | | |
| Turn-on Delay Time[2] | $T_{d(on)}$ | - | 11.5 | - | ns | $V_{DS}$=20V<br>$I_D$=1A<br>$V_{GS}$=10V<br>$R_G$=3.3<br>$R_D$=20 |
| Rise Time | $T_r$ | - | 6.3 | - | | |
| Turn-off Delay Time | $T_{d(off)}$ | - | 28.2 | - | | |
| Fall Time | $T_f$ | - | 12.6 | - | | |
| Input Capacitance | $C_{iss}$ | - | 1725 | - | pF | $V_{GS}$=0V<br>$V_{DS}$=25V<br>f=1.0MHz |
| Output Capacitance | $C_{oss}$ | - | 235 | - | | |
| Reverse Transfer Capacitance | $C_{rss}$ | - | 145 | - | | |

## Source-Drain Diode

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Forward On Voltage[2] | $V_{SD}$ | - | - | 1.3 | V | $I_S$=2.3A, $V_{GS}$=0V, Tj=25℃ |
| Continuous Source Current (Body Diode) | $I_S$ | - | - | 2.3 | A | $V_D$= $V_G$=0V, $V_S$=1.3V |
| Pulsed Source Current (Body Diode)[1] | $I_{SM}$ | - | - | 20 | A | |

Notes: 1. Pulse width limited by Max. junction temperature.

2. Pulse width≦300us, duty cycle≦2%.

3. Surface mounted on 1 $in^2$ copper pad of FR4 board; 135℃/W when mounted on min. copper pad.

## Characteristics Curve

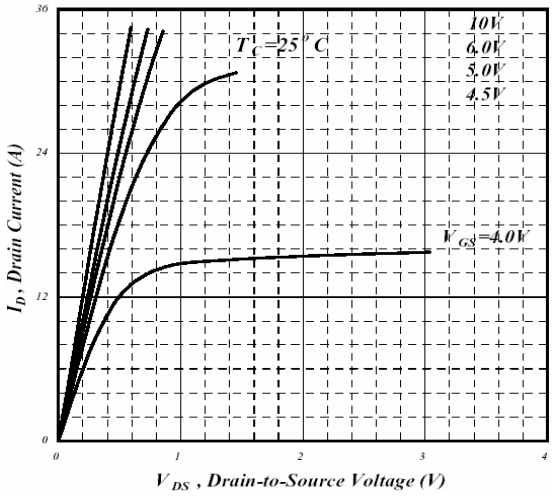



**Fig 1. Typical Output Characteristics**

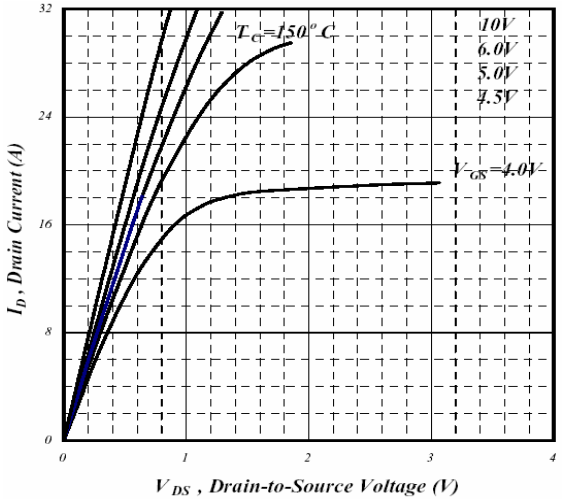



**Fig 2. Typical Output Characteristics**

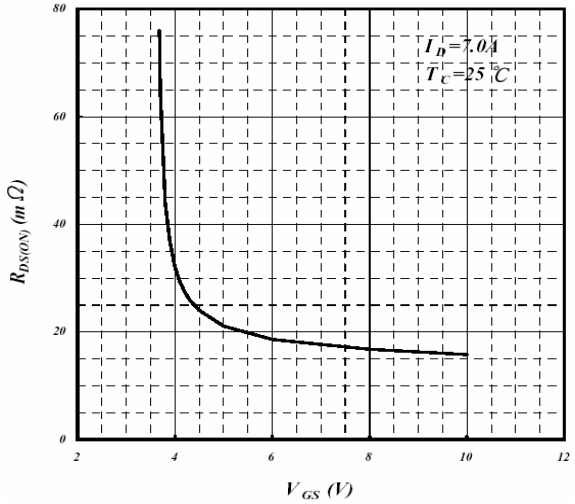



**Fig 3. On-Resistance v.s. Gate Voltage**

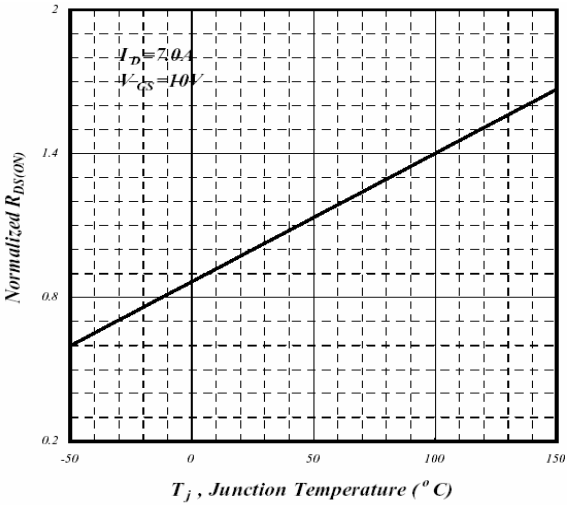



**Fig 4. Normalized On-Resistance v.s. Junction Temperature**

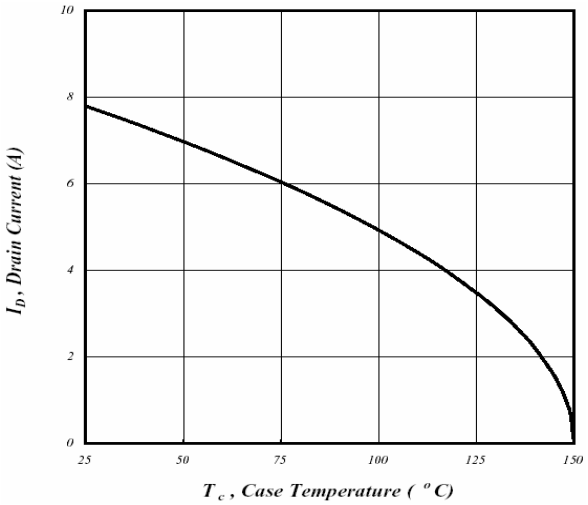



**Fig 5. Maximum Drain Current v.s. Case Temperature**

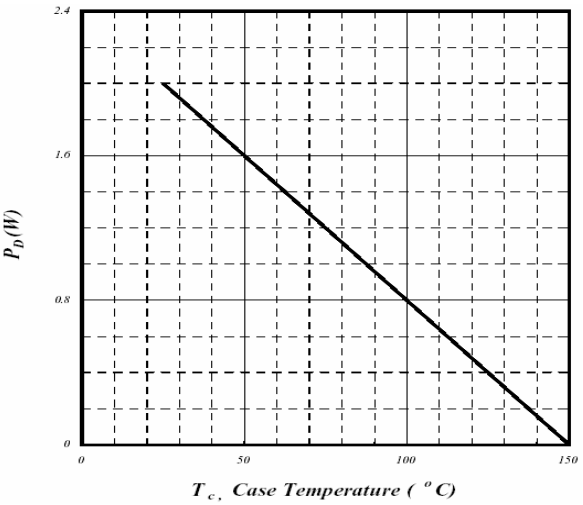



**Fig 6. Type Power Dissipation**

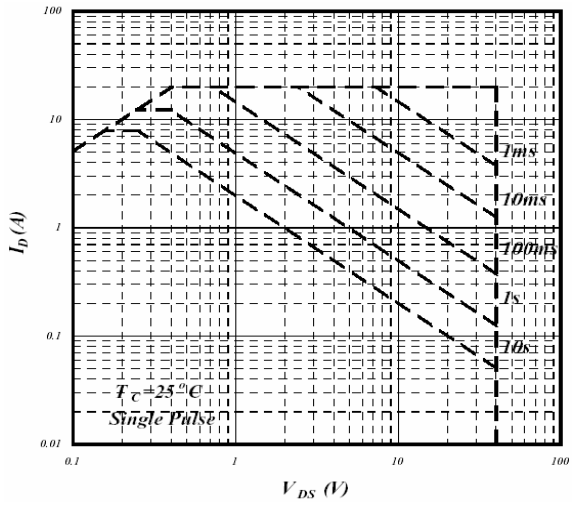



**Fig 7. Maximum Safe Operating Area**

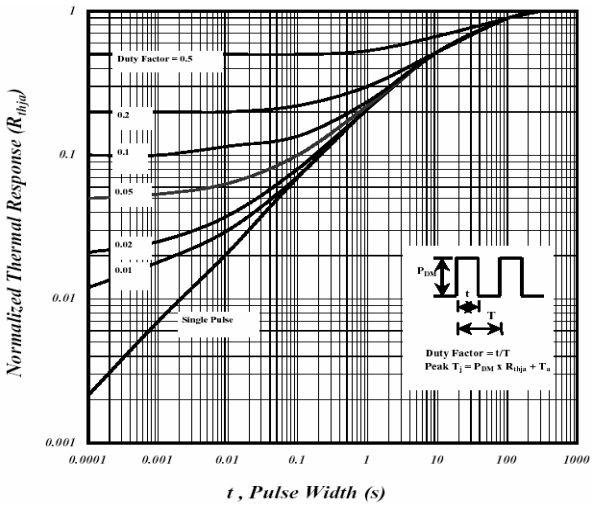



**Fig 8. Effective Transient Thermal Impedance**

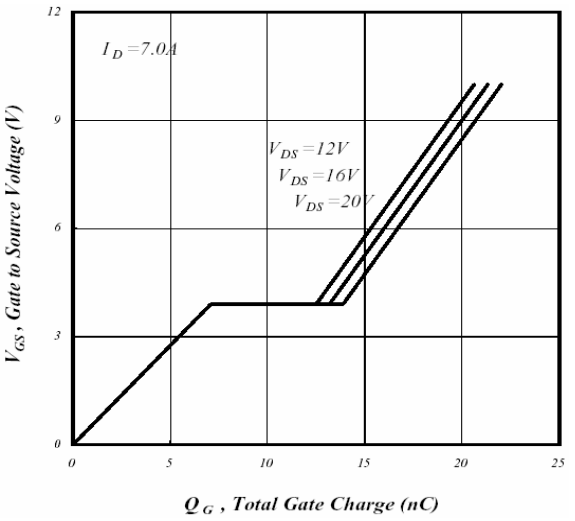



**Fig 9. Gate Charge Characteristics**

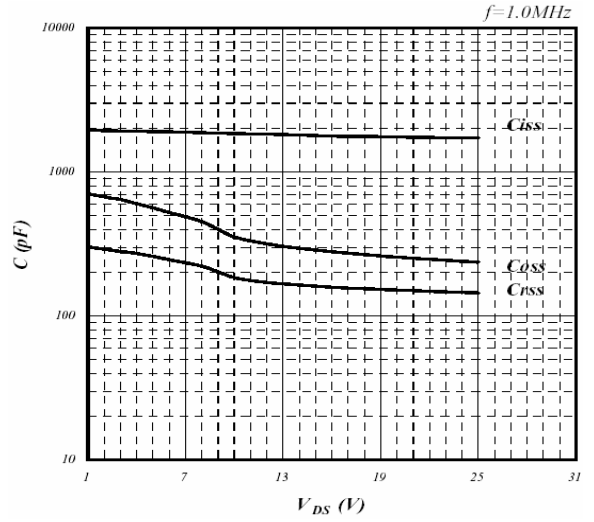



**Fig 10. Typical Capacitance Characteristics**

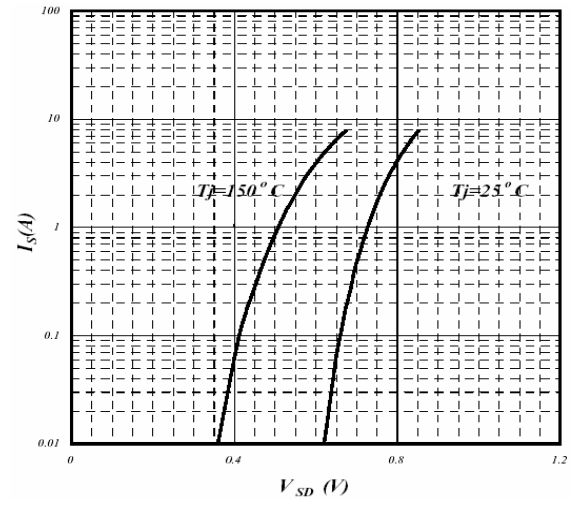



**Fig 11. Forward Characteristics of Reverse Diode**

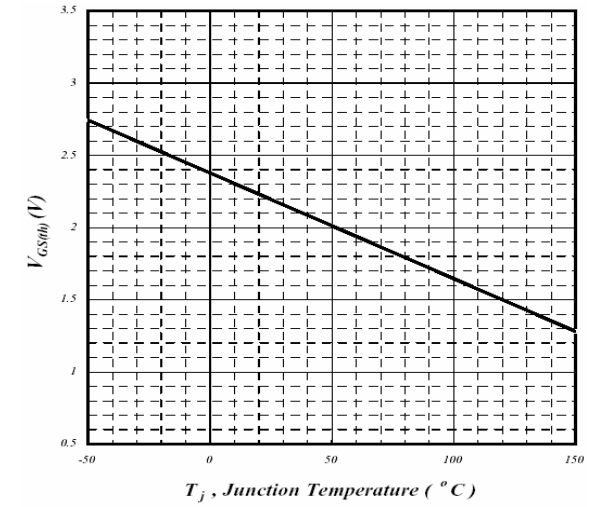



**Fig 12. Gate Threshold Voltage v.s. Junction Temperature**

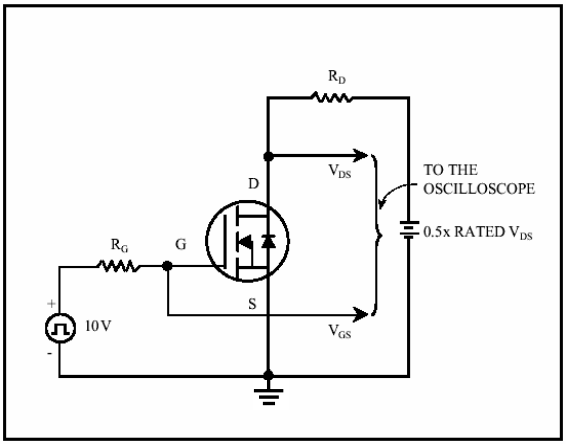



Fig 13. Switching Time Circuit

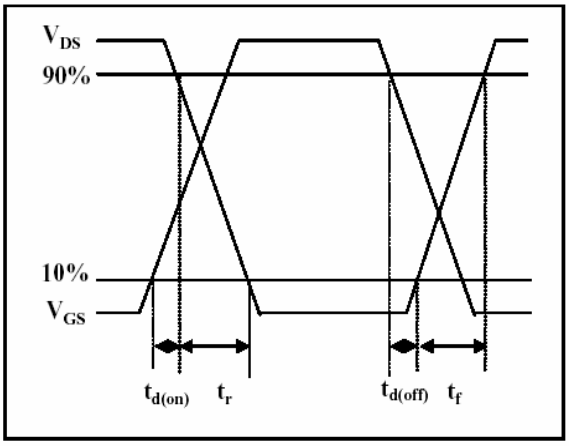



Fig 14. Switching Time Waveform

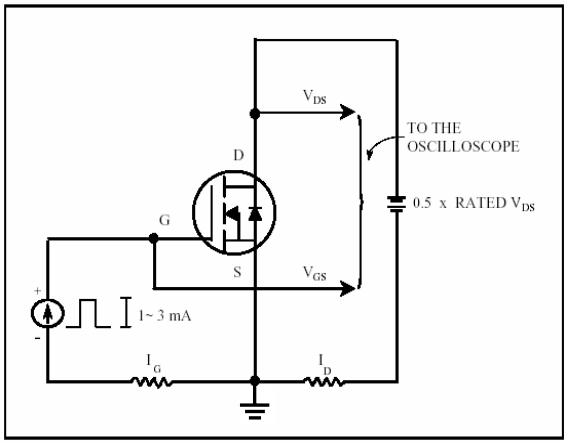



Fig 15. Gate Charge Circuit

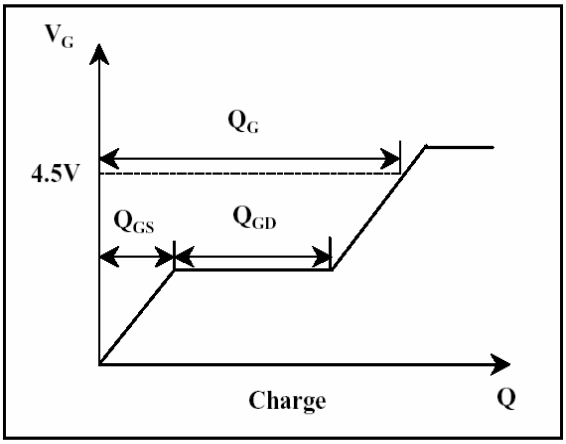



Fig 16. Gate Charge Waveform